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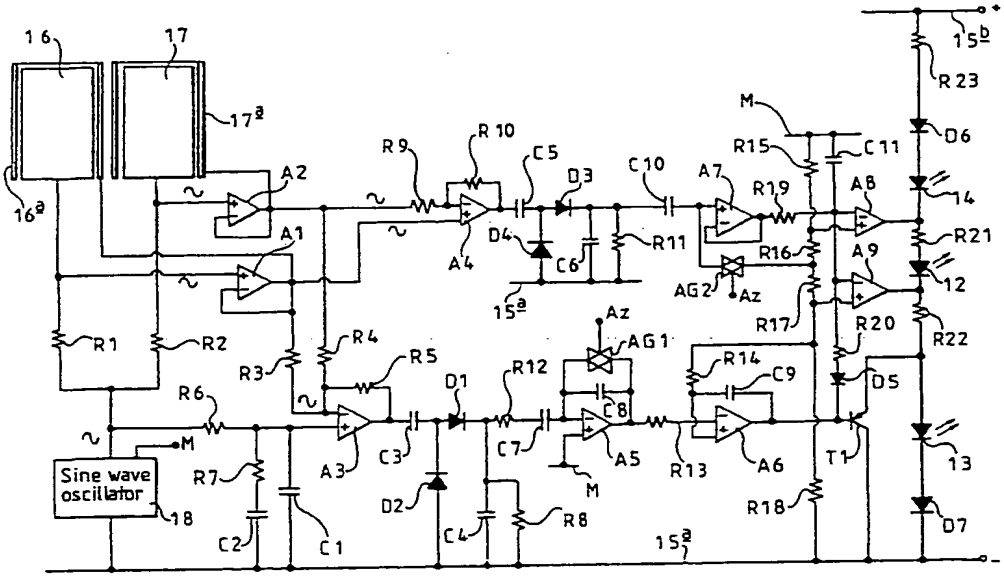

(57) Abstract

A detector device for finding concealed studs in partitioning includes a pair of plates (16, 17) which are supplied with ac via resistors (R_1 and R_2). Amplifiers (A_3 and A_4) produce outputs representing the sum and difference respectively of the signals imposed on the plates. The sum signal drives a display enabling circuit including a comparator (A_6) which enables a display means to operate when the sum signal exceeds a threshold level. The difference signal drives two comparators (A_8 and A_9) which control three display devices (12, 13 and 14) such that one display device (12) is operated only when the detector device is over the centre of a stud. The other display devices indicate which way the detector should be moved to place it over the centre of the stud.

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DEVICE FOR FINDING CONCEALED STUDS

This invention relates to a device for finding concealed studs in hollow partitions and the like.

Stud finding devices utilising capacitive detectors are already known, e.g. from GB-B-2159630. The device described in that document makes use of a capacitor plate to which an oscillator output is applied. The device is moved over a partition containing studs and provides a display dependent on the effective capacitance of the capacitor plate. An automatic self calibrating arrangement is employed to allow the device to be set up over a part of the partition where there is no underlying stud.

The known device has the disadvantage that it is not easy to use it to find the centre of a concealed stud. The display indicates that the capacitance rises relatively rapidly as the capacitor plate starts to overlap the stud and remains at a maximum level over a considerable area. It is thus necessary for the user to note the limits of the maximum capacitance area and estimate its centre.

It is an object of the present invention to provide a device which makes finding of the centre of a concealed stud relatively simple.

In accordance with the invention there is provided a device for detecting the position of a stud in a partition comprising first and second substantially coplanar side-by-side capacitor plates which are electrically isolated from one another, means for applying an alternating signal to said plates through first and second impedance means respectively, so as to produce on said plates alternating voltage signals of amplitude related to the capacitance of each plate, means for producing a first electrical

signal related to the sum of such alternating voltage signals, means for producing a second electrical signal related to the difference between such alternating voltage signals and display means including display enabling means operable in accordance with said first electrical signal and balance indicating means operable in accordance with said second electrical signal.

The display means may include three display devices operating when the display is enabled to indicate respectively (a) when the first capacitor plate has a significantly higher capacitance than the second, (b) when the capacitances of the two plates are substantially equal and (c) when capacitance of the second plate is significantly higher than that of the first.

The three display devices, which may be light emitting diodes, are preferably arranged to indicate the direction in which the device must be moved to achieve balance.

The device preferably has a self-calibrating arrangement arranged to establish a threshold level for the sum signal and a balance level for the difference signal during initial operation of the device.

An example of the invention is shown in the accompanying drawings in which:

Figure 1 is an elevation of a device in accordance with the invention;

Figure 2 is a circuit diagram of the device;

Figure 3 is a circuit diagram of a switch-on pulse circuit and a voltage regulator forming part of the device;

Figure 4 is a graph showing voltage signals produced in the circuit of Figure 2 and their variation with the position of the device relative to a detected stud;

Figure 5 is a block diagram for a device in accordance with a second embodiment of the invention;

Figures 6 and 7 are two halves of a circuit diagram corresponding to the block diagram of Figure 5;

Figure 8 is a graph similar to that of Figure 4, for the second embodiment of the invention; and

Figures 9 and 10 are block diagrams for third and fourth embodiments of the invention respectively, each also including a schematic graph of the type shown in Figure 4.

Referring to Figure 1, the device shown has a case 10 with a switch operating element 10^b mounted on it at one side. In the front face of the case 10, there are mounted four light emitting diodes 11, 12, 13 and 14 in a diamond shaped layout, one of these leds 12 being green and triangularly shaped. One vertex of the triangle is directed towards a notch 10^a in the end of the case. The remaining leds are red.

Contained within the casing is an operating circuit which includes a battery 15 and a pair of rectangular, coplanar capacitor plates 16, 17,

formed as areas of a printed circuit board (not shown). This board lies close to the back face of the casing.

Turning now to Figure 2 it will be seen that plates 16 and 17 are connected by respective ones of two resistors R_1 and R_2 to the output terminal of a sine wave oscillator 18. A pair of buffer amplifiers A_1 and A_2 have their non-inverting inputs connected to the respective plates 16 and 17. Each amplifier A_1 and A_2 has a direct feedback connection from its output to its inverting input. Each capacitor plate 16, 17, is substantially surrounded by a printed circuit track 16^a, 17^b and these are connected respectively to the outputs of the two amplifiers A_1 and A_2 so that these two tracks are maintained at the same voltage as the respective capacitor plates, but are driven from the low impedance outputs of the amplifiers, rather than through the high impedance paths provided by the resistors R_1 and R_2.

The buffer amplifiers A_1, A_2 provide signals determined by the voltages on the two plates 16, 17 both to a summing amplifier A_3 and to a difference amplifier A_4. Two resistors R_3 and R_4 connect the outputs of amplifiers A_1 and A_2 to the inverting input of amplifier A_3, negative feedback around amplifier A_3 being provided by a resistor R_5. The resistance values are chosen to provide a gain of 5 of each input signal. The non-inverting input of amplifier A_3 is connected by a resistor R_6 to the output of the oscillator 18 and by a capacitor C_1 connected in parallel with the series combination of a resistor R_7 and another capacitor C_2 to the battery negative rail 15^a. The components R_6, R_7, C_2 and C_1 are chosen to provide a signal corresponding to the sum of the outputs of amplifiers A_1 and A_2 when the device is operated in free space.

The input of amplifier A_3 is connected to a rectifying circuit comprising an input capacitor C_3 connected to the anode of a diode D_1 and the cathode of a diode D_2. The anode of diode D_2 is connected to the rail 15^a and the cathode of diode D_1 is connected by a capacitor C_4 to rail 15^a. A resistor R_8 is connected across the capacitor C_4. Capacitor C_4 has a capacitance of about 10 times that of capacitor C_3 so that the rectifier acts as a diode pump to charge up capacitor C_4 to a peak voltage related to the amplitude of the sum signal at the output of amplifier A_3, charge being allowed to leak away through resistor R_8 when the amplitude falls.

The difference amplifier A_4 has its non-inverting input connected to the output of buffer amplifier A_1 and its inverting input connected by a resistor R_9 to the output of buffer amplifier A_2. Negative feedback is provided by a resistor R_{10}, of ohmic value chosen to give a gain of 10. A rectifying circuit similar to the one described above is connected to the output of amplifier A_4. This rectifier circuit comprises diodes D_3 and D_4, capacitors C_5 and C_6 and a resistor R_{11}. The diode D_4, the capacitor C_2 and the resistor R_{11} are connected to the rail 15^a.

The output of the sum signal rectifying circuit, taken from the cathode of diode D_1, is connected via a resistor R_{12} and a capacitor C_7 in series to the inverting input of an operational amplifier A_5 which has negative feedback provided by a capacitor C_8 and which has its non-inverting input connected to a regulated voltage rail M. A CMOS analog gate element AG_1 is connected in parallel with the capacitor C_8 for discharging capacitor C_8 and providing direct boot strapping of amplifier A_5 during automatic self-calibration as will be hereinafter described.

The output of amplifier A_5 is connected by a resistor R_{13} to the inverting input of another operation amplifier A_6. This has its non-inverting input connected by a resistor R_{14} to a point on a voltage divider chain R_{15}, R_{16}, R_{17} and R_{18} connected between the rail M and the rail 15ª. Positive feedback around amplifier A_6 is provided by a capacitor C_9.

The output of the difference signal rectifying circuit, taken from the cathode of the diode D_3 is connected by a capacitor C_{10} to the non-inverting input of another operational amplifier A_7 connected as a voltage follower. Another analog gate AG_2 connects another point on the voltage divider chain to the non-inverting input of amplifier A_7 for self-calibration.

The resistor chain R_{15} ... R_{18} has relatively high ohmic value resistors R_{15} and R_{18} at opposite ends and two relatively low ohmic value resistors R_{16}, R_{17} in between. The common point of resistors R_{15} and R_{16} is connected to the non-inverting input of an operational amplifier A_8 and the common point of resistors R_{17} and R_{18} is connected to the non-inverting input of an operational amplifier A_9. The common point of resistors R_{16} and R_{17} is connected to analog gate AG_2. The inverting inputs of amplifiers A_8 and A_9 are connected to one another, to the output of amplifier A_7 by a resistor R_{19}, to the rail M by a capacitor C_{11} and to the output of amplifier A_6 by a resistor R_{20} and a diode D_5 in series. The latter connection ensures that the outputs of amplifiers A_8 and A_9 (which act as voltage comparators) both go high when the output of amplifier A_6 goes low irrespective of the output of amplifier A_7.

The green triangular led 12 is connected in series with a resistor R_{21} between the outputs of amplifiers A_8 and A_9. The led 13 has its anode

connected by a resistor R_{22} to the output of amplifier A_9 and its cathode connected by a diode D_8 to the rail 15^a. The led 14 is connected in series with a diode D_6 and a resistor R_{23} between the positive battery rail 15^b and the output of amplifier A_8.

The circuit shown in Figure 2 is completed by a pnp transistor T_1 which has its base connected to the output of amplifier A_6 and its collector-emitter connected across led 13.

Figure 3 shows a switch 19 which is operated by the element 10^b and which connects the rail 15^b to the battery positive terminal. Figure 3 also shows a start up pulse circuit including an analog gate device AG_3. Device AG_3 is connected at one side to rail 15^a and at the other side by a resistor R_{24} to rail 15^b, a diode 11 being included in the series circuit. Device AG_3 has its control terminal connected by a resistor R_{25} to rail 15^a and by a capacitor C_{12} to rail 15^b so that it is switched on only while capacitor C_{12} is charging up following closing of switch 19. The led 11 remains on when the device AG_3 is conducting.

Figure 2 includes an operational amplifier A_{10} which has its non-inverting input connected to the rail 15^a by a 3v zener diode D_8. The inverting input of amplifier A_{10} is connected to rail 15^a by a resistor R_{26}. Negative feedback is provided by a resistor R_{27} and a resistor R_{28} connected between the output of amplifier A_{10} and the cathode of the zener diode D_8 provides current to the latter. A smoothing capacitor C_{12} is connected between the output of amplifier A_{10} and rail 15^a.

In operation, the device is held against a partition to be tested and the switch 19 is closed. The oscillator and all the operational amplifiers are

powered up immediately and gates AG_1 and AG_2 are both turned on. This causes the non-inverting input of amplifier A_7 to be held at a specific voltage for a period so that capacitor C_{10} charges to a voltage determined by the difference voltage signal. Similarly capacitor C_7 charges to a voltage determined by the sum signal voltage. Throughout the continuing operation (i.e. for a few seconds) capacitors C_{10} and C_7 hold these voltages, thereby providing the required automatic self calibration operation.

On termination of the power on pulse, the sum and difference voltage signals vary in dependence on the dielectric constants of material over which the plates 16 and 17 lie, as the device is moved along the partition surface. When a stud in the partition is encountered, the amplitude of the alternating voltage on the first plate to encounter the stud starts to rise first. This causes the sum voltage to rise and the difference voltage to rise or fall depending on which plate has encountered the stud. Whilst the sum voltage is below a threshold value, the output of amplifier A_6 is low, thereby turning on transistor T_1 and causing the outputs of both amplifiers A_8 and A_9 to go high, ensuring that none of the leds is lit. When the sum rises above this threshold value amplifier A_6 output goes high. At this stage the outputs of both amplifiers A_8 and A_9 will be the same, either high or low depending on which plate has encountered the stud first. Thus either led 13 or led 14 is lit. As the balance point is approached, the output voltage of amplifier A_7 enters the narrow band of voltages over which it lies between the voltages on the non-inverting inputs of amplifiers A_8 and A_9. Thus green led 12 alone is lit. As movement continues, the A_7 output voltage again goes outside the narrow band causing the other of leds 13 or 14 to be lit.

When the green led is on, the partition may be marked by means of a pencil in notch 10^a to indicate the stud centre.

With reference to Figures 5, 6 and 7 the sine wave oscillator 18 is a Colpitts type oscillator which is formed by transistors Q_1 and Q_2 and the associated components including capacitors C_1 and C_2 and inductor L_1 which determine the frequency of oscillation. Power is supplied to the oscillator by means of a voltage regulator which is based upon integrated circuit UIC and zener diode ZI.

As in the example of Figure 2, the detector plates are supplied with the sine wave signal from the oscillator by way of resistors R_8 and R_9 respectively and associated with the plates and the associated shields, are FET input buffer amplifiers U2A and U2D. The outputs of the amplifiers are connected to peak detection circuits each formed by a diode and a capacitor. The signals at the points SL and SR in Figure 6 are therefore the peak levels of the signals from the respective plates minus the diode volt drop.

The signals at the points SL and SR are applied to a difference amplifier U2B and a summing amplifier U2C. The difference amplifier has associated close tolerance resistors having values such that the gain is 10. If there is any error in the resistor values common mode signals will appear at the output and a low pass filter formed by resistor R13 and capacitor C8 is provided. The filter has a -3dB cut off at 15.9Hz.

Figure 7 shows the portion of the circuit which is concerned with the display and reset and is coupled to the portion of the circuit shown in

Figure 6 by the connections indicated at the right hand of Figure 6 and the left hand of Figure. 7.

The calibration stage acts to eliminate any offset in the outputs of the sum and difference amplifiers U2C and U2B. The stage utilizes a quad CMOS switch U4 which is provided with an RC circuit formed by capacitor C7 and resistor R19. At switch on the capacitor is discharged so that inputs CONA-COND are at logic "I" and all the CMOS switches are closed. As the capacitor is charged the voltage applied to the input falls and eventually the inputs reach logic "o" so that the switch is switched off.

The difference amplifier output may have an offset and this is effectively removed by the action of capacitor C4 and U3B which has a high impedance FET input. This input is shorted by the action of the CMOS switch to the junction of R24 and R25 forming part of the LED display driver. Any offset is therefore removed and when the CMOS switch is turned off the input of U3B is free to respond to the output of the difference amplifier.

The summing amplifier is zeroed using a high impedance FET operational amplifier U3A which at switch on has its output connected to its inverting input by the CMOS switch. The amplifier thus acts as a voltage follower and its inverting input assumes the voltage of its non-inverting input. As a result one plate of the capacitor C9 is held at 3U5 and the other plate is held at a potential determined by the offset of the summing amplifier. When the CMOS switches open, the capacitor C9 holds the offset voltage and the amplifier U3A operates as an inverting amplifier with a gain of 10. Capacitor C10 acts to remove any low

frequency interference which may appear at the output of the summing amplifier.

The output of the amplifier U3A is utilized to enable the LED display when approaching a stud or batten. The LED display is a simple window detector which corresponds closely with that shown in Figure 2.

Figure 8 shows the voltage variations which take place as the detector moves towards and beyond a batten.

Figures 9 and 10 show block diagrams of alternative detectors.

Although the description above refers to studs and battens in partitions, other position detection operations could readily be carried out using an appropriately designed embodiment of the invention.

CLAIMS

1. A device for detecting the position of a stud in a partition comprising first and second substantially coplanar side-by-side capacitor plates which are electrically isolated from one another, means for applying an alternating signal to said plates through first and second impedance means respectively, so as to produce on said plates alternating voltage signals of amplitude related to the capacitance of each plate, means for producing a first electrical signal related to the sum of such alternating voltage signals, means for producing a second electrical signal related to the difference between such alternating voltage signals and display means including display enabling means operable in accordance with said first electrical signal and balance indicating means operable in accordance with said second electrical signal.

2. A device as claimed in Claim 1, in which said display means includes three display devices operating when the display is enabled to indicate respectively (a) when the first capacitor plate has a significantly higher capacitance than the second, (b) when the capacitances of the two plates are substantially equal and (c) when capacitance of the second plate is significantly higher than that of the first.

3. A device as claimed in Claim 2, in which said display devices are connected in series with a plurality of resistors between a pair of supply terminals and said display means further comprises a pair of comparators having inputs connected to said difference signal means and to points on a reference resistor chain and outputs connected to points on the series circuit including said display devices so as to cause said

display devices to be selectively energised as specified when the display enabling means is operating to enable display.

4. A device as claimed in Claim 3, wherein said display enabling means comprises a further comparator having inputs connected to compare the output of said sum signal means with a reference voltage with its output connected to inputs of said pair of comparators and to a switching device for shorting one of the display devices when the sum signal is less than the reference voltage.

5. A device as claimed in Claim 3, in which said difference signal means comprises a difference amplifier having inputs connected to said plates and a first rectifier circuit connected to the output of said difference amplifier and providing a dc output dependent on the amplitude of the output of said difference amplifier.

6. A device as claimed in Claim 5, in which the output of said first rectifier circuit is connected to said pair of comparators via a first automatic calibration circuit comprising a voltage follower having its input connected by a capacitor to the output of said first rectifier circuit and via a first calibration switch device to a reference voltage source, said first calibration switch device being conductive for an initial period each time the device is actuated.

7. A device as claimed in Claim 4, in which said sum signal means comprises a summing amplifier having inputs connected to said plates and a second rectifier circuit connected to the output of said summing amplifier and providing a dc output dependent on the amplitude of the output of said difference amplifier.

8. A device as claimed in Claim 7, in which the output of said second amplifier is connected to said further comparator via a second automatic calibration circuit comprising an integrating amplifier ac coupled to said rectifier output and including a feedback capacitor and a second calibration switch device connected across said feedback capacitor, said second calibration switch device being conductive for an initial period each time the device is actuated.

9. A device as claimed in Claim 3, in which said difference signal means comprises a difference amplifier having inputs connected to peak detection circuits respectively, said peak detection circuits being supplied with said alternating current signals respectively.

10. A device as claimed in Claim 3, in which said sum signal means comprises a summing amplifier having inputs connected to peak detection circuits respectively, said peak detection circuits being supplied with said alternating current signals respectively.

11. A device as claimed in Claim 9 or Claim 10 including buffer amplifiers through which the alternating current signals are supplied to said peak detection circuits.

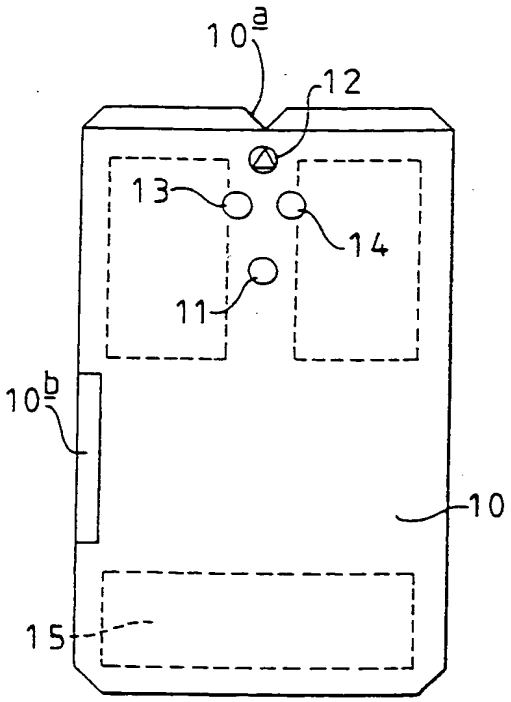


FIG 1

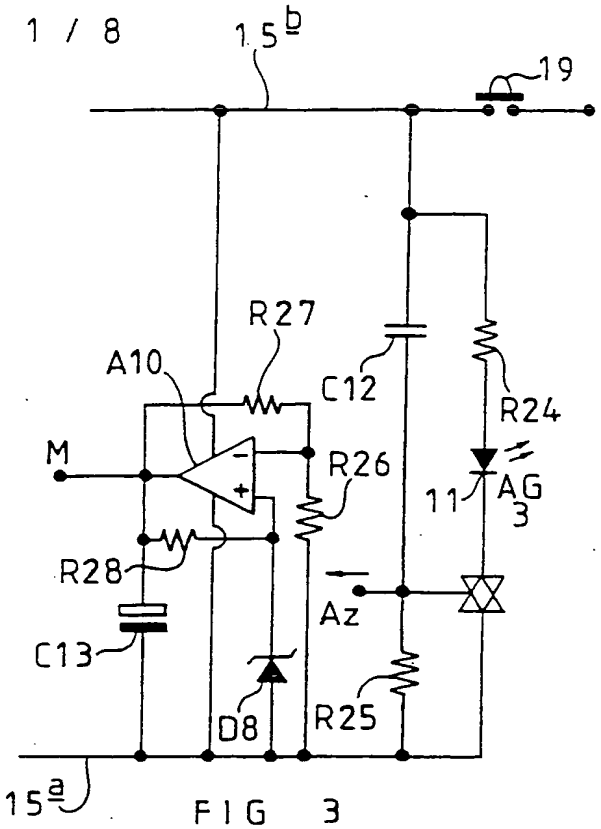
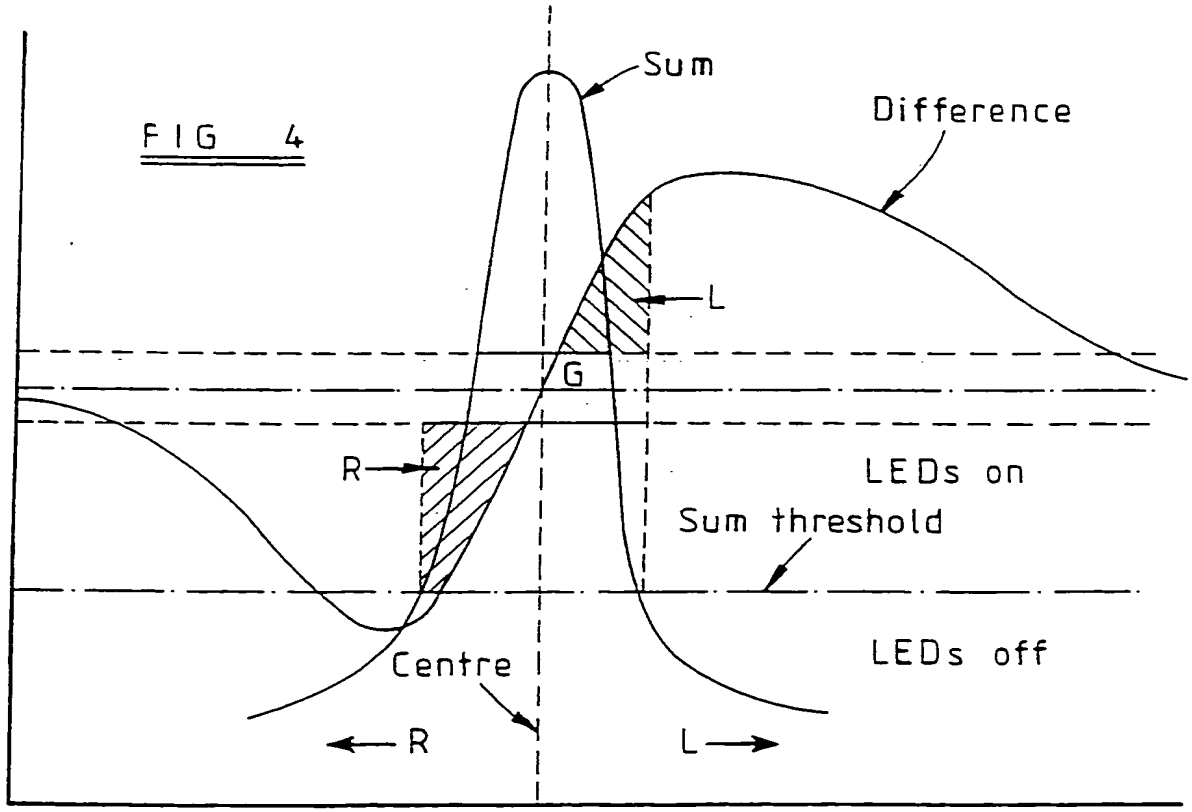


FIG 3

FIG 4



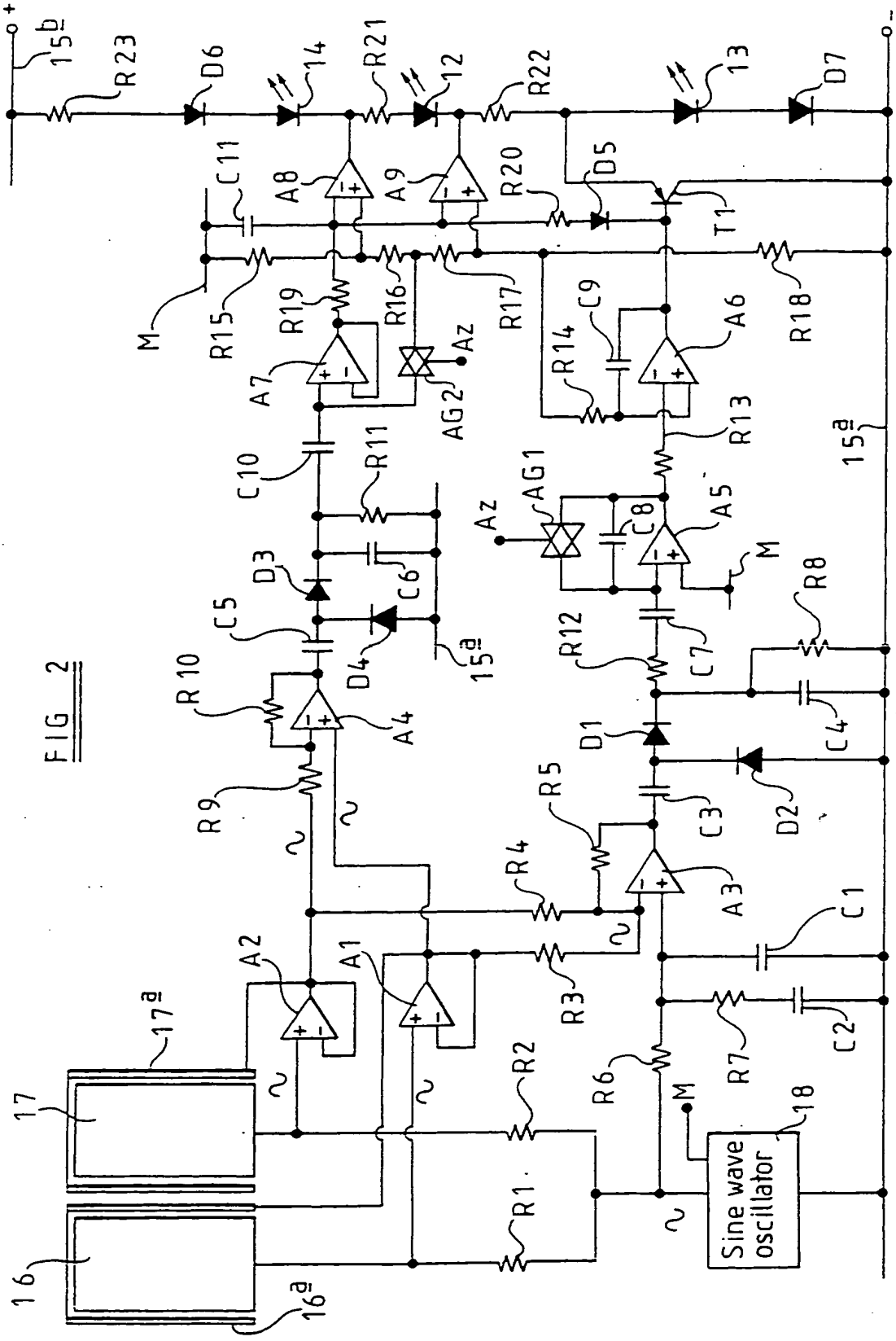

+
15b
R23
D6
14
R21
12
R22
13
D7
C11
A8
A9
R20
D5
T1
M
R15
R19
R16
R17
C9
A6
R18
A7
Az
AG2
R14
C10
R11
R13
15a
AG1
Az
A5
C8
M
D3
C6
C5
R8
R12
C7
D4
15a
R10
A4
C4
D1
D2
R9
R5
C3
R4
A3
C1
A2
A1
R3
17a
R2
C2
R7
17
R6
M
18
Sine wave oscillator
R1
16
16a

FIG 2

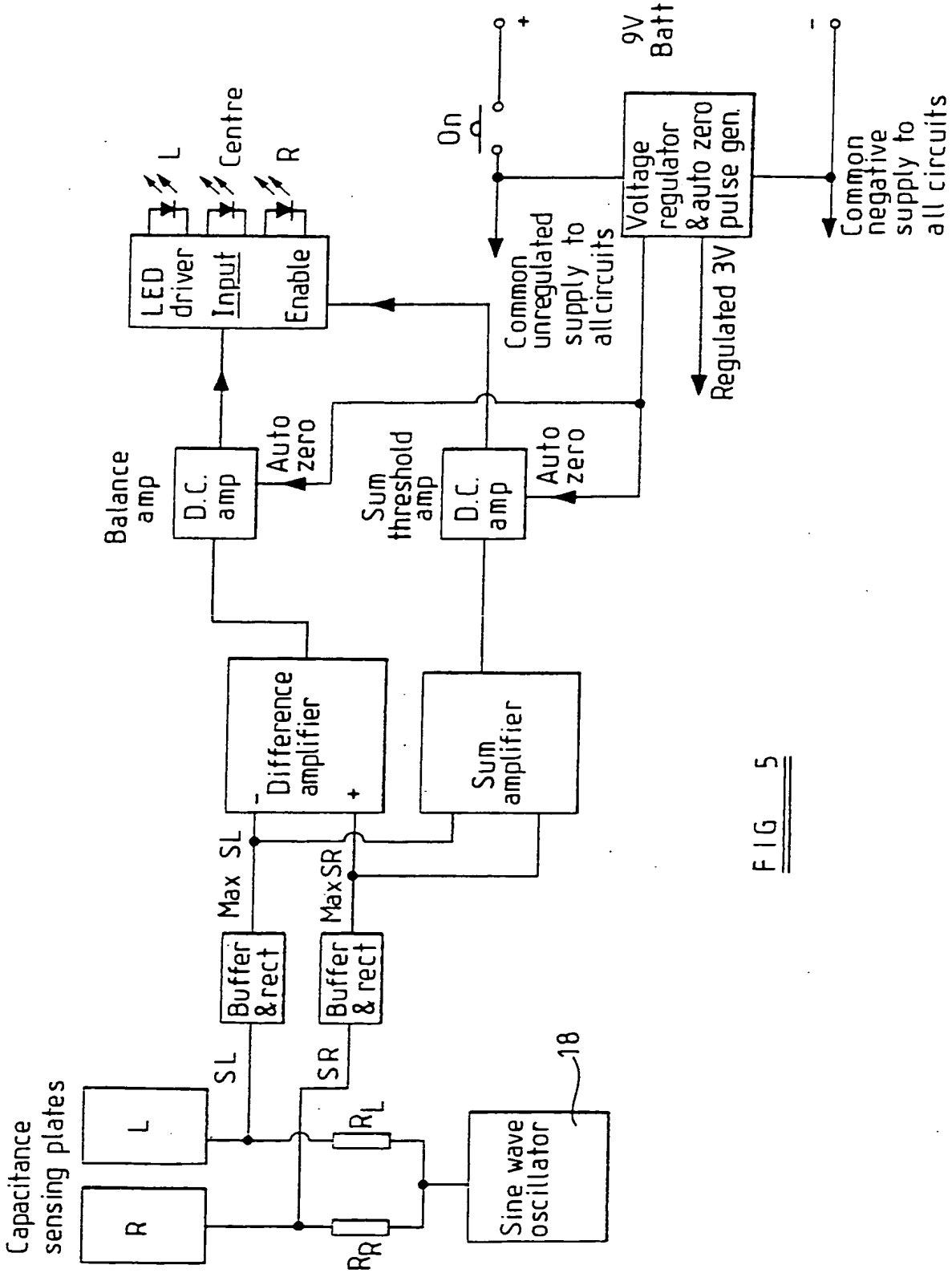

9V Batt
+
-
On
Voltage regulator & auto zero pulse gen.
Common negative supply to all circuits
Regulated 3V
Common unregulated supply to all circuits
L
Centre
R
LED driver
Input
Enable
Balance amp
D.C. amp
Auto zero
Sum threshold amp
D.C. amp
Auto zero
Difference amplifier
Sum amplifier
Max SL
MaxSR
Buffer & rect
Buffer & rect
SL
SR
Capacitance sensing plates
L
R
R_L
R_R
Sine wave oscillator
18

FIG 5

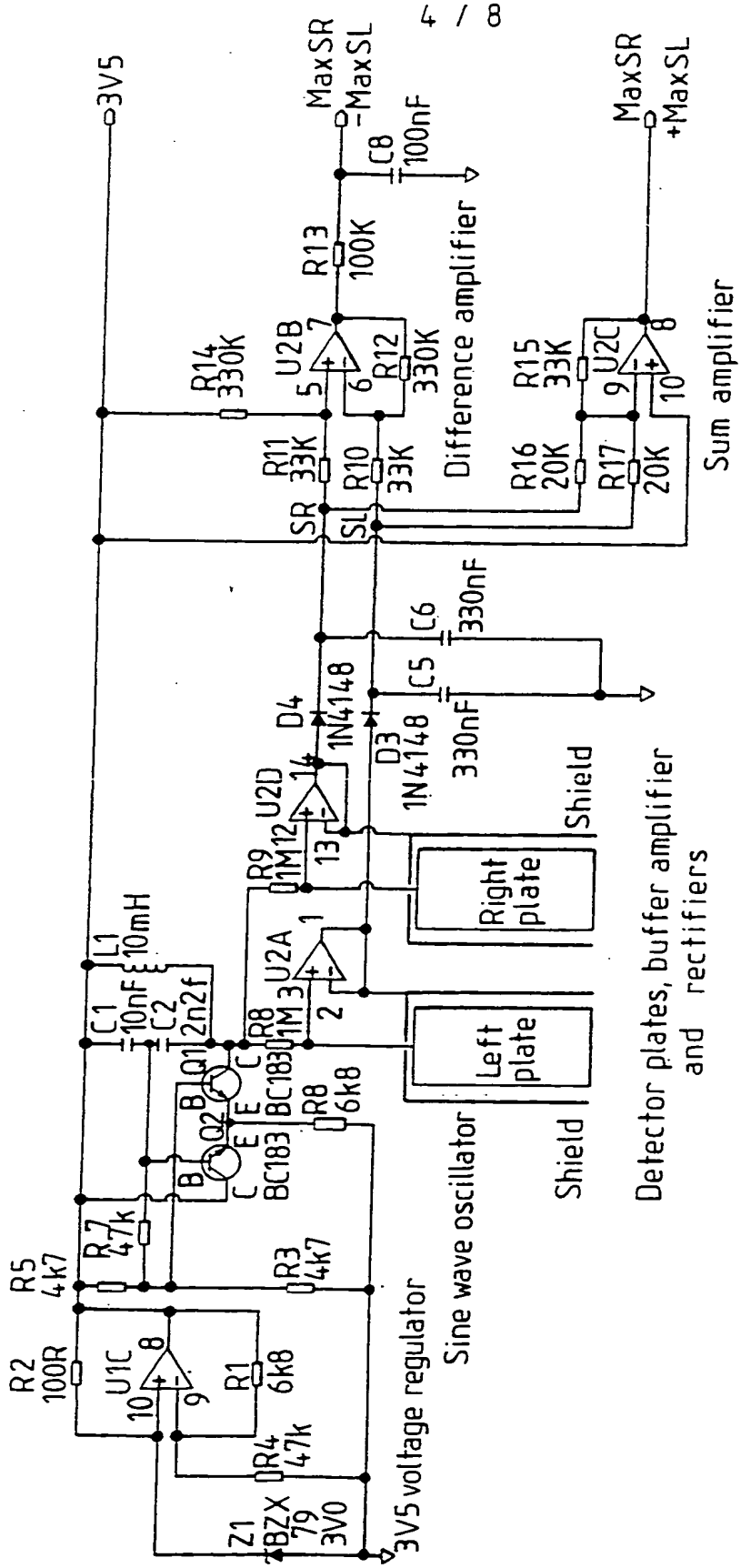

3V5
MaxSR
-MaxSL
C8
100nF
R13
100K
U2B
R14
330K
R12
330K
Difference amplifier
R11
33K
R10
33K
SR
SL
R15
33K
U2C
R16
20K
R17
20K
Sum amplifier
MaxSR
+MaxSL
C6
330nF
C5
330nF
D4
1N4148
D3
1N4148
U2D
R9
1M
R8
1M
U2A
L1
10mH
C1
10nF
C2
2n2f
Q1
BC183
Q2
BC183
R8
6k8
R7
47k
R5
4k7
R3
4k7
R2
100R
U1C
R1
6k8
R4
47k
Z1
BZX
79
3V0
3V5 voltage regulator
Sine wave oscillator
Left
plate
Right
plate
Shield
Shield
Detector plates, buffer amplifier
and rectifiers

FIG 6

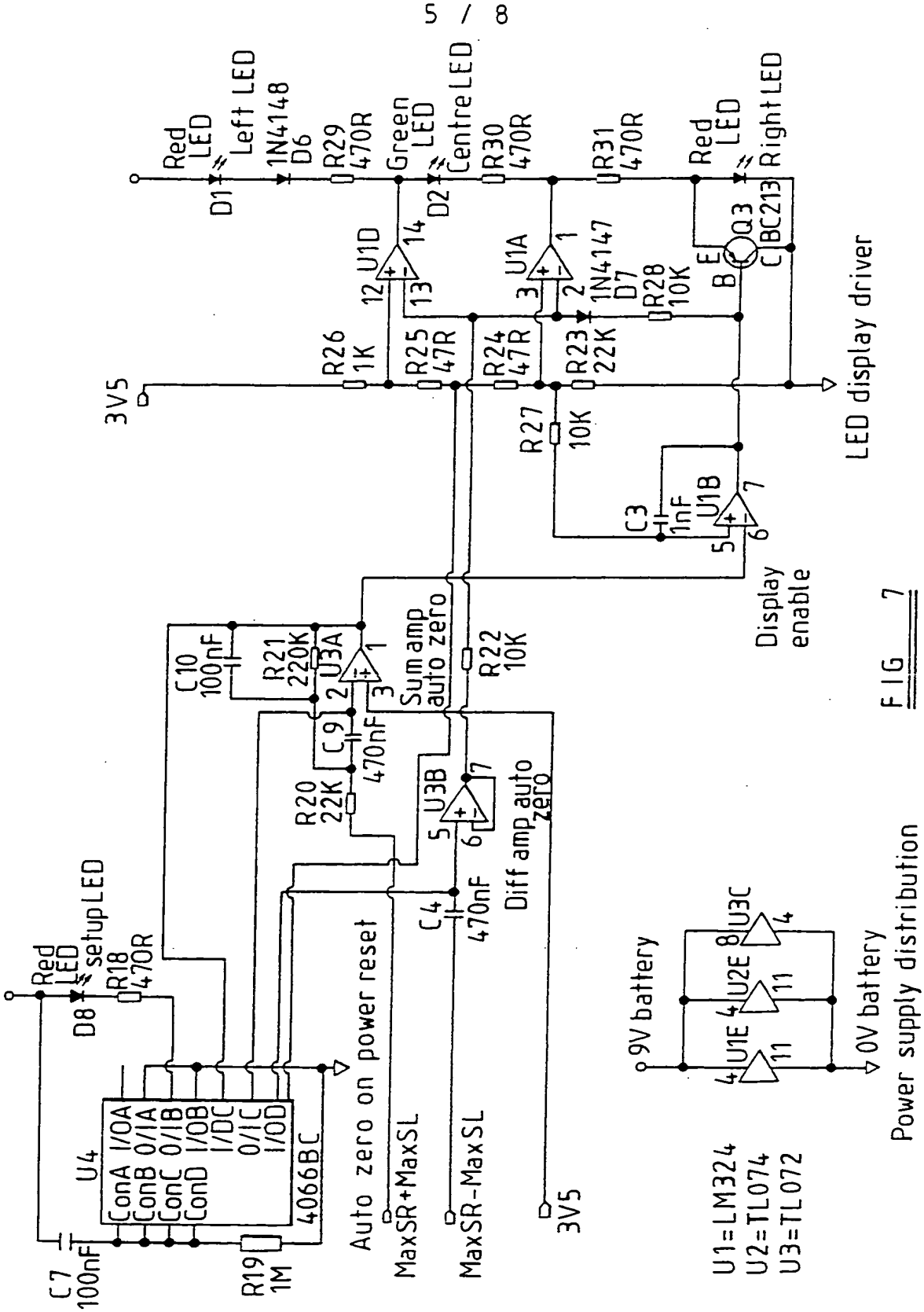

Red LED D1
Left LED 1N4148 D6
R29 470R
Green LED D2
Centre LED
R30 470R
R31 470R
Red LED
Right LED
U1D
U1A
1N4147 D7
R28 10K
Q3 BC213
LED display driver
3V5
R26 1K
R25 47R
R24 47R
R23 22K
R27 10K
C3 1nF
U1B
Display enable
C10 100nF
R21 220K
U3A
Sum amp auto zero
R22 10K
C9 470nF
R20 22K
U3B
Diff amp auto zero
C4 470nF
Red LED D8
setup LED
R18 470R
U4
4066BC
C7 100nF
R19 1M
Auto zero on power reset
MaxSR+MaxSL
MaxSR-MaxSL
3V5
9V battery
U2E
U1E
U3C
0V battery
Power supply distribution
U1=LM324
U2=TL074
U3=TL072

FIG 7

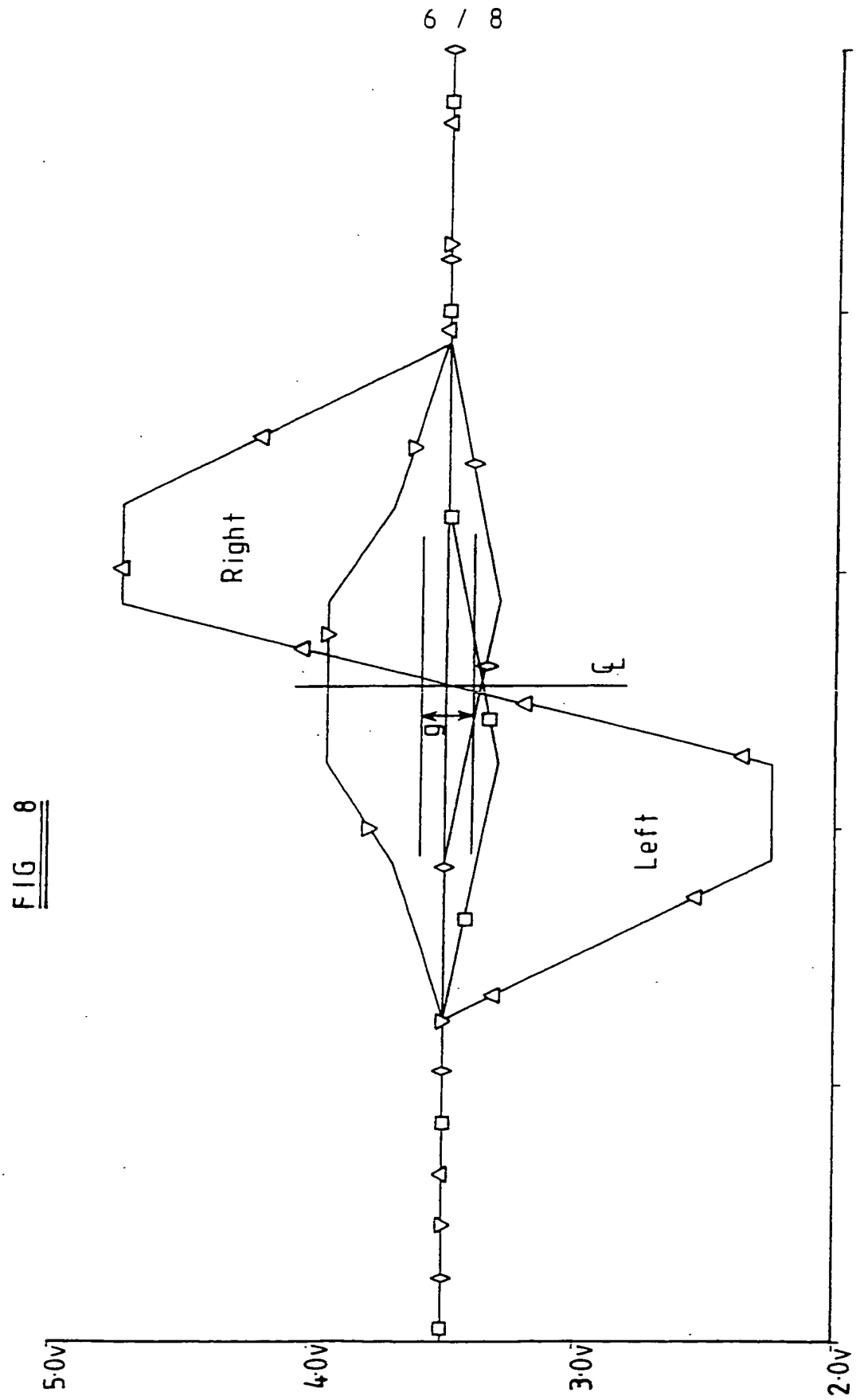

Right
Left
g
5·0v
4·0v
3·0v
2·0v
□V(R8:1) ◇V(V3:+) ▽V(U2:out) △V(U1:out)
SL SR SUM DIFF.
Time

FIG 8

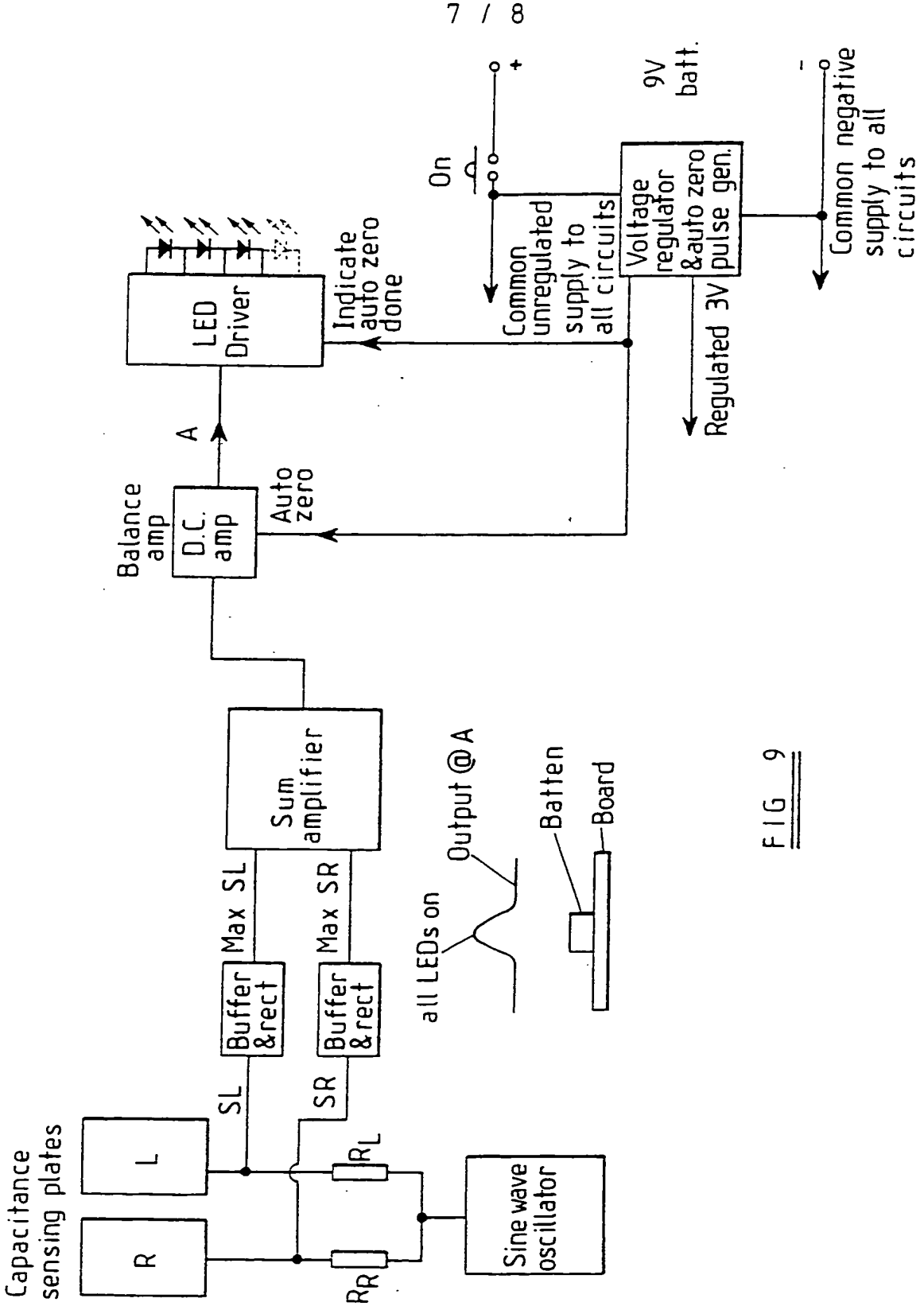

Capacitance sensing plates
L
R
SL
SR
R_L
R_R
Sine wave oscillator
Buffer &rect
Buffer &rect
Max SL
Max SR
Sum amplifier
Balance amp
D.C. amp
Auto zero
A
LED Driver
Indicate auto zero done
Common unregulated supply to all circuits
On
+
9V batt.
Voltage regulator &auto zero pulse gen.
Regulated 3V
-
Common negative supply to all circuits
Output @A
all LEDs on
Batten
Board

FIG 9

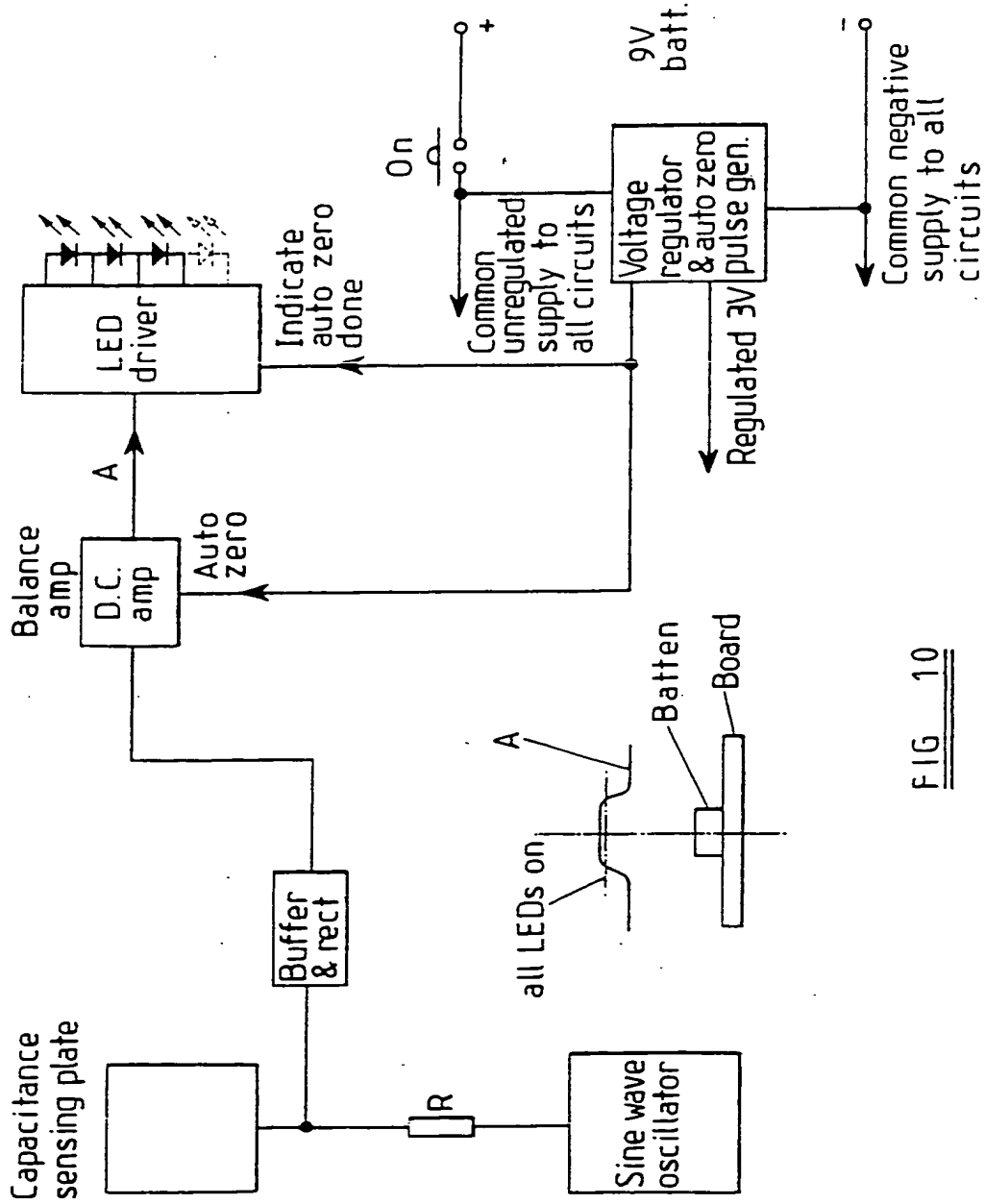

Capacitance sensing plate
Sine wave oscillator
R
Buffer & rect
Balance amp
D.C. amp
A
Auto zero
LED driver
Indicate auto zero done
Common unregulated supply to all circuits
On
+
9V batt.
Voltage regulator & auto zero pulse gen.
Regulated 3V
-
Common negative supply to all circuits
A
all LEDs on
Batten
Board

FIG 10

INTERNATIONAL SEARCH REPORT

Intern ial Application No
PCT/GB 95/00489

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01V3/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01V

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB,A,2 159 630 (FRANKLIN ROBERT CHARLES) 4 December 1985 cited in the application see abstract	1
A	US,A,4 191 894 (NODA MASAHIRO ET AL) 4 March 1980 see abstract; figure 2	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 June 1995	05. 07. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Anderson, A

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INTERNATIONAL SEARCH REPORT

information on patent family members

Interr al Application No
PCT/GB 95/00489

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
GB-A-2159630	04-12-85	US-A-	4464622	07-08-84
		AU-A-	1231983	15-09-83
		GB-A,B	2117909	19-10-83
		JP-A-	58171690	08-10-83
US-A-4191894	04-03-80	JP-C-	1148883	26-05-83
		JP-A-	53063582	07-06-78
		JP-B-	57041169	01-09-82
		FR-A,B	2371676	16-06-78

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